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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Andrew Marshall, et al.	Docket No:	TI-31157
Serial No:	10/023,113	Conf. No:	2385
Examiner:	Khiem D. Nguyen	Art Unit:	2823
Filed:	12/13/2001		

For: MEMORY CELL WITH TRANSISTORS HAVING RELATIVELY HIGH THRESHOLD VOLTAGES IN RESPONSE TO SELECTIVE GATE DOPING

APPEAL BRIEF UNDER 37 C.F.R. 1.192

MAILING CERTIFICATE UNDER 37 C.F.R. §1.8(A)
I hereby certify that this Appeal Brief filed, in triplicate, under 37 CFR 1.192 is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on 2-17-04.

Ann Trent
Ann Trent

Mail Stop Appeal Brief - Patents
Commissioner For Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The following Appeal Brief is respectfully submitted in triplicate and in connection with the above identified application in response to the final rejection mailed November 10, 2003, and the Advisory Action mailed December 23, 2003.

Real Party in Interest under 37 C.F.R. 1.192(c)(1)

Texas Instruments Incorporated is the real party in interest.

Related Appeals and Interferences under 37 C.F.R. 1.192 (c)(2)

There are no related appeals or interferences known to appellant, the appellant's legal representative, or assignee which will directly affect or be directly affected by or have a bearing on the board's decision in the pending appeal.

Status of Claims on Appeal under 37 C.F.R. 1.192 (c)(3)

Claims 1-22 were filed. Claims 1-22 were rejected and are appealed.

Status of Amendments Filed After Final rejection under 37 C.F.R. 1.192 (c)(4)

No amendments were filed after the Final rejection under 37 C.F.R. 1.192(c)(4).

Summary of the Invention under 37 C.F.R. 1.192(c)(5)

The instant invention describes a method for forming a memory cell/circuit comprising transistors having relatively high threshold voltages in response to selective gate doping. The invention is best illustrated by referencing Figures 2(a) – 2(c). Figure 2(a) shows ST1 and NT1 regions in a p-type semiconductor where MOS transistors will be formed. In Fig. 2(b), the polysilicon layer 28 in region NT1 is selectively implanted while the polysilicon layer 28 in the ST1 region is selectively masked by the mask layer 30. As shown in Figure 2(c), MOS transistors are formed in region ST1 and NT1. The source drain regions 34_1 and 34_2 for the ST1 transistor and the source drain regions 36_1 and 36_2 for the NT1 transistor are of the same conductivity type (page 14, lines 18-21). During this process additional dopants are introduced into the polysilicon region 28_2. It should be noted that the polysilicon region 28_2 has a different concentration of dopants compared to polysilicon region 28_3 due in part to the additional implant process shown in Fig. 2(b).

Statement of Issues Presented for Review under 37 C.F.R. 1.192 (C)(6)

Are claims 1-20 properly rejected under U.S.C. 102(e) as being anticipated by Nishihara et al. (U.S. Pub. 2002/0137320)?

Statement of the Grouping of Claims under 37 C.F.R. 1.192(C)(7)

Claims 1-20 stand or fall together.

Arguments

Are claims 1-20 properly rejected under U.S.C. 102(e) as being anticipated by Nishihara et al. (U.S. Pub. 2002/0137320)?

Appellants contend that claims 1-20 are not properly rejected under U.S.C. 102(e) as being anticipated by Nishihara et al. (U.S. Pub. 2002/0137320).

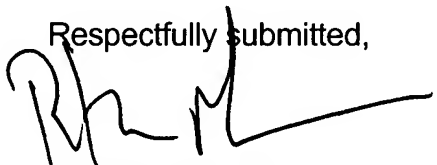
Claims 1 and 17, and 20 of the instant invention comprises the limitations of the fourth doped region and the third doped region being of the same conductivity type as the first and second doped regions. The claims further comprise the limitations of forming the first gate with a first doping concentration between the first and second doped regions and the second gate with a second doping concentration between the third and fourth doped regions such that the second doping concentration is different from the first doping concentration. In rejecting claim 1 the examiner refers to the Nishihara patent and in particular to regions 14 in Figures 1-7 as being equivalent to the first and second doped region and region 13 on the left side as being equivalent to the third and fourth doped region. The examiner is referred to page 5, paragraph [0079], where the formation of these regions is described. Region 13 is described as p+ and region 14 is described as n+. These are different conductivity types and do not fall within the limitation of claim 1. In addition all the 8n gate regions have the same doping and all the 8p have the same doping as they are all formed simultaneously as described in paragraph [0079]. The different gate doping requirement of claim 1 is not found in the cited art. Claims 1, 17 and 20 are allowable over the cited art. In addition claims 2-16, 18-20, and 21-22 depend on claims 1, 17 and 20 respectively and contain the limitations of these claims. Therefore claims 2-16, 18-20, and 21-22 are also allowable over the cited art.

Conclusion

For the foregoing reasons, Appellants respectfully submit that the Examiner's final rejection of Claims 1-22 under 35 U.S.C. § 102 is not properly founded in law, and it is respectfully requested that the Board of Patent Appeals and Interferences so find and reverse the Examiner's rejections.

To the extent necessary, the Appellants petition for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668. **This form is submitted in triplicate.**

Respectfully submitted,



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APPENDIX

Claims on Appeal

1. A method of forming a semiconductor circuit, comprising the steps of:

forming a first transistor, comprising the steps of:

forming a first source/drain region as a first doped region in a fixed relationship to a semiconductor substrate;

forming a second source/drain region as a second doped region in a fixed relationship to the semiconductor substrate, wherein the second doped region and the first doped region are of a same conductivity type; and

forming a first gate in a fixed relationship to the first source/drain region and the second drain region; and

forming a second transistor, comprising the steps of:

forming a third source/drain region as a third doped region in a fixed relationship to the semiconductor substrate;

forming a fourth source/drain region as a fourth doped region in a fixed relationship to the semiconductor substrate, wherein the fourth doped region and the third doped region are of the same conductivity type as the first and second doped regions;

forming a second gate in a fixed relationship to the third source/drain region and the fourth drain region; and

wherein the steps of forming the first gate and the second gate comprise forming the first gate to comprise a first dopant concentration and forming the second gate to comprise a second dopant concentration different from the first dopant concentration.

2. The method of claim 1 wherein the steps of forming the first and the second gate further comprise:

forming a semiconductor layer in a fixed relationship to the semiconductor substrate;

in an implant step, selectively implanting dopants into a portion of the semiconductor layer in an area corresponding to the first transistor while not implanting dopants into a portion of the semiconductor layer in an area corresponding to the second transistor.

3. The method of claim 2 wherein the steps of forming the first gate and the second gate further comprise patterning and etching the semiconductor layer to form the first gate from the area corresponding to the first transistor and the second gate from the area corresponding to the second transistor.

4. The method of claim 2 wherein the semiconductor layer comprises polysilicon.

5. The method of claim 4 wherein the step of forming a semiconductor layer comprises forming a polysilicon layer with an in-situ doping.

6. The method of claim 5:

wherein the in-situ doping comprises p-type in-situ doping; and

wherein the first, second, third, and fourth doped regions comprise n-type doped regions.

7. The method of claim 2:

wherein the first transistor has a first threshold voltage in response to the first dopant concentration; and

wherein the second transistor has a second threshold voltage in response to the second dopant concentration and such that the second threshold voltage is greater than the first threshold voltage.

8. The method of claim 7 wherein the second transistor comprises a state transistor in a memory cell.

9. The method of claim 8:

wherein the state transistor comprises a first state transistor;

and further comprising the step of forming a second state transistor in the memory cell, comprising the step of forming a third gate corresponding to the second state transistor and comprising the second dopant concentration.

10. The method of claim 9 and further comprising the steps of:

forming a first access transistor in the memory cell, the first access transistor coupled and operable to read a state from, and write a state to, a source/drain of the first state transistor; and

forming a second access transistor in the memory cell, the second access transistor coupled and operable to read a state from, and write a state to, a source/drain of the second state transistor.

11. The method of claim 10 wherein the first and second access transistors comprise source/drain regions of a conductivity type that is complementary of source/drain regions of the first and second state transistors.

12. The method of claim 11 wherein the first, second, third, and fourth doped regions comprise n-type doped regions.

13. The method of claim 12:

wherein the semiconductor layer comprises polysilicon; and

wherein the step of forming a semiconductor layer comprises forming a polysilicon layer with an in-situ doping.

14. The method of claim 12 wherein the first transistor comprises a transistor in a sense amplifier.

15. The method of claim 8 wherein the first transistor comprises a transistor in a sense amplifier.

16. The method of claim 15 wherein the first, second, third, and fourth doped regions comprise n-type doped regions.

17. A method of forming a memory configuration, comprising the steps of:

forming a plurality of memory cells, wherein each of the memory cells is formed comprising the step steps of:

forming a first transistor, comprising the steps of:

forming a first source/drain region as a first doped region in a fixed relationship to a semiconductor substrate;

forming a second source/drain region as a second doped region in a fixed relationship to the semiconductor substrate, wherein the second doped region and the first doped region are of a same conductivity type; and

forming a first gate in a fixed relationship to the first source/drain region and the second drain region; and

forming a second transistor outside of the plurality of memory cells, comprising the steps of:

forming a third source/drain region as a third doped region in a fixed relationship to the semiconductor substrate;

forming a fourth source/drain region as a fourth doped region in a fixed relationship to the semiconductor substrate, wherein the fourth doped region and the third doped region are of the same conductivity type as the first and second doped regions;

forming a second gate in a fixed relationship to the third source/drain region and the fourth drain region; and

wherein, the step of forming the first gate for each cell in the plurality of memory cells and the step of forming the second gate further comprise:

forming a semiconductor layer in a fixed relationship to the semiconductor substrate; and

in an implant step, selectively implanting dopants into a portion of the semiconductor layer in an area corresponding to the second transistor such that the area has a first dopant concentration while not implanting dopants into a portion of the semiconductor layer in an area corresponding to the first transistor in each cell.

18. The method of claim 17:

wherein, for each cell, the first transistor has a first threshold voltage in response to the implant step; and

wherein the second transistor has a second threshold voltage in response to the first dopant concentration and such that the second threshold voltage is less than the first threshold voltage.

19. The method of claim 18:

wherein the first transistor comprises a first state transistor;

and further comprising the step of forming a second state transistor in the memory cell, comprising the step of forming a third gate corresponding to the second state transistor and wherein the implant step further comprises selectively implanting dopants into a portion of the semiconductor layer while not implanting dopants into a portion of the semiconductor layer in an area corresponding to the second state transistor in each cell.

20. The method of claim 19 and further comprising the steps of:

forming a first access transistor in the memory cell, the first access transistor coupled and operable to read a state from, and write a state to, a source/drain of the first state transistor; and

forming a second access transistor in the memory cell, the second access transistor coupled and operable to read a state from, and write a state to, a source/drain of the second state transistor.

21. A semiconductor circuit, comprising:

a first transistor, comprising:

a first source/drain region comprising a first doped region in a fixed relationship to a semiconductor substrate;

a second source/drain region comprising a second doped region in a fixed relationship to the semiconductor substrate, wherein the second doped region and the first doped region are of a same conductivity type; and

a first gate in a fixed relationship to the first source/drain region and the second drain region; and

a second transistor, comprising:

a third source/drain region comprising a third doped region in a fixed relationship to the semiconductor substrate;

fourth source/drain region comprising a fourth doped region in a fixed relationship to the semiconductor substrate, wherein the fourth doped region and the third doped region are of the same conductivity type as the first and second doped regions;

a second gate in a fixed relationship to the third source/drain region and the fourth drain region; and

wherein the first gate comprises a first dopant concentration and the second gate comprises a second dopant concentration different from the first dopant concentration.

22. A memory configuration comprising:

a plurality of memory cells, wherein each of the memory cells comprises:

a first transistor, comprising:

a first source/drain region comprising a first doped region in a fixed relationship to a semiconductor substrate;

a second source/drain region comprising a second doped region in a fixed relationship to the semiconductor substrate, wherein the second doped region and the first doped region are of a same conductivity type; and

a first gate in a fixed relationship to the first source/drain region and the second drain region; and

the memory configuration further comprising a second transistor outside of the plurality of memory cells, comprising:

a third source/drain region comprising a third doped region in a fixed relationship to the semiconductor substrate;

a fourth source/drain region comprising a fourth doped region in a fixed relationship to the semiconductor substrate, wherein the fourth doped region and the third doped region are of the same conductivity type as the first and second doped regions;

a second gate in a fixed relationship to the third source/drain region and the fourth drain region; and

wherein the first gate for each cell in the plurality of memory cells comprises a first dopant concentration that is less than a dopant concentration in the second gate.